WHAT IS CLAIMED IS:

1. A method for producing a semiconductor wafer with semiconductor dies for electronic components, the method comprising:

providing a semiconductor wafer, arranged in rows and columns, with semiconductor die positions,

creating an active surface area in the semiconductor die positions on an active top side of the semiconductor wafer and applying contact connecting areas outside the active surface area,

applying and patterning a sacrificial layer which comprises insulation material, on the active surface area, leaving through openings in the sacrificial layer exposed in the edge areas of the active surface area,

applying a conductive material to the sacrificial layer and into the through openings for forming a cover layer with through lines,

removing the sacrificial layer by forming a self-supporting cover layer, supported by through lines, above a hollow space above the active surface area,

applying and patterning a first plastic layer on the cover layer and on the active top side, leaving the contact connecting areas exposed and sealing side edges of the hollow space above the active surface area,

applying external contacts to the contact connecting areas, and

splitting the semiconductor wafer into individual electronic components.

2. The method as claimed in claim 1, wherein the sacrificial layer is deposited on the semiconductor wafer from a chemical gas phase, forming silicon oxide or silicon nitride, or as a photoresist layer on the semiconductor wafer.

3. The method as claimed in claim 1, wherein, after a cover layer comprising a polycrystalline silicon has been applied, a sacrificial layer comprising silicon oxide is removed by hydrofluoric acid.

4. The method as claimed in claim 1, wherein, after a metallic cover layer of nickel, copper, aluminum or alloys thereof has been applied, a sacrificial layer comprising photoresist is removed by a solvent.

5. The method as claimed in claim 4, wherein, onto the first plastic layer a rewiring pattern is applied which connects the contact connecting areas to external contact areas and then a second plastic layer is applied, leaving the external contact areas exposed.

6. The method as claimed in claim 1, wherein, onto the first plastic layer a rewiring pattern is applied which connects the contact connecting areas to external contact areas and then a second plastic layer is applied, leaving the external contact areas exposed.

7. An electronic component comprising a semiconductor die, the semiconductor die comprising:

a semiconductor substrate,

an active top side on the semiconductor substrate,

an active surface area on the active top side,

contact connecting areas electrically connected to the active surface area,

a package comprising a package-forming plastic layer which covers the substrate leaving the contact connecting areas exposed, and

a self-supporting electrically conductive cover layer which is arranged above the active surface area and which is supported on through lines to the active top side and forms a hollow space between the active surface area and cover layer,

wherein the height of the hollow space corresponds to the thickness of an insulation layer, photoresist layer or metal layer for a semiconductor wafer.

8. The electronic component as claimed in claim 7, wherein the cover layer has a thickness which corresponds to a thickness of conductor tracks on a semiconductor wafer.

9. The electronic component as claimed in claim 7, wherein the contact connecting areas are arranged outside the active surface area and comprise external contacts of the electronic component.

10. The electronic component as claimed in claim 7, wherein the package-forming plastic layer covers the cover layer, leaving the contact connecting areas exposed, and seals the hollow space on the side between the through lines.

11. The electronic component as claimed in claim 7, further comprising a first plastic layer on which a rewiring pattern with rewiring lines is arranged which lead from the contact connecting areas to external contact areas, external contacts being arranged on the external contact areas, and a second plastic layer is arranged on the first plastic layer, leaving the external contacts exposed and embedding the rewiring pattern.

12. The electronic component as claimed in claim 11, wherein the through lines are arranged regularly distributed around the circumference of the cover layer.

13. The electronic component as claimed in claim 7, wherein the through lines are arranged regularly distributed around the circumference of the cover layer.

14. The electronic component as claimed in claim 7, wherein the cover layer comprises a metal or a semiconductor material.

15. The electronic component as claimed in claim 14, wherein the metal or semiconductor material is heavily doped polycrystalline silicon.

16. The electronic component as claimed in claim 7, wherein the semiconductor die contains a filter circuit, the filter circuit being implemented using film bulk acoustic resonators.

17. A semiconductor wafer comprising electronic components arranged in rows and columns, each electronic component comprising a semiconductor die, the semiconductor die comprising:

a semiconductor substrate,

an active top side on the semiconductor substrate,

an active surface area on the active top side,

contact connecting areas electrically connected to the active surface area,

a package comprising a package-forming plastic layer which covers the substrate leaving the contact connecting areas exposed, and

a self-supporting electrically conductive cover layer which is arranged above the active surface area and which is supported on through lines to the active top side and forms a hollow space between the active surface area and cover layer,

wherein the height of the hollow space corresponds to the thickness of an insulation layer, photoresist layer or metal layer for a semiconductor wafer.

18. A semiconductor wafer as claimed in claim 17 further comprising conductor tracks, the cover layer having a thickness which corresponds to the thickness of the conductor tracks.

19. A semiconductor wafer as claimed in claim 17, wherein the contact connecting areas are arranged outside the active surface area and comprise external contacts of the electronic component.

20. A semiconductor wafer as claimed in claim 17, further comprising a first plastic layer on which a rewiring pattern with rewiring lines is arranged which lead from the contact connecting areas to external contact areas, external contacts being arranged on the external contact areas, and a second plastic layer is arranged on the first plastic layer, leaving the external contacts exposed and embedding the rewiring pattern.